REMARKS

The Application has been carefully reviewed in light of the Office Action dated December 28, 2004. Claims 1 to 18 are in the application, of which Claims 1, 11, 17 and 18 are independent. Claims 1, 5, 12, 17 and 18 are being amended. Reconsideration and further examination are respectfully requested.

Initially, Applicant gratefully acknowledges the indication that Claims 17 and 18 recite patentable subject matter, and that Claims 9, 10, 13 and 14 would be allowable if rewritten in independent form. Since it is Applicant's strong belief that the claims from which these claims depend are also allowable, Claims 9, 10, 13 and 14 are not being rewritten in independent form.

Claims 1 to 8, 11, 12, 15 and 16 have been rejected under 35 U.S.C. §103(a) over U.S. Patent 5,357,152 (Jennings), U.S. Patent 6,112,019 (Chamdani) and U.S. Patent No. 5,491,694 (Oliver). Reconsideration and withdrawal of the rejection are respectfully requested for the reasons set forth below.

The present invention generally concerns a computer processor comprising a plurality of processing units each of which are interconnected via a communication bus. An important feature of the present invention is that the communication means which interconnects the plurality of processing units includes a common bus, over which packetized information may be communicated. In a first configuration arranged by the communication means, the processing unit may have a larger number of the processing units arranged in parallel than in a second configuration also arranged by the dynamically-configurable communication means, and the second configuration may have a deeper pipeline depth than the first configuration.

By virtue of this arrangement, communication paths for packetized information between the processing units can be selectively arranged to suit the nature of the processing, such that has the requirements of processing change, the configuration of the processing units can be adapted to suit the changing requirements.

Turning to the specific language of the claims, Claim 1 defines a computer processor comprising a plurality of processing units and a communication means. The communication means includes a common bus to which each of the plurality of processing units are interconnected for communication of packetized information over the common bus. The communication means is dynamically configurable based on a processing of a computer program to thereby selectively arrange communication paths for the packetized information between the processing units in at least first and second distinct configurations, the first distinct configuration having a larger number of the processing units arranged in parallel than the second distinct configuration, and the second distinct configuration having a deeper pipeline depth than the first distinct configuration.

The applied art, namely Jennings, Chamdani and Oliver, is not seen to disclose or to suggest the above features, particularly as regards a computer processor comprising a plurality of processing units and a communication means which includes a common bus to which each of a plurality of processing units are interconnected for communication of packetized information over the bus, the communication means being dynamically configurable based on a processing of a computer program to selectively arrange communication paths for packetized information between the plurality of processing units over a common bus in at least two distinct configurations.

At page 2, the Office Action states that Jennings' programmable circuit and

its configurable signal bus LSF and LSC (in Figure 2 of Jennings) is the same as the claimed dynamically-configurable communication means. The Office Action continues and states that the integer and floating point selections described at col. 7, lines 36 to 40 and col. 5, lines 1 to 27 disclose the claimed distinct configurations.

While the programmable circuit of Jennings is configured to deliver control signals to each of the processing units so that a processing unit can modify its operation to achieve a different result, this is not seen to be the same as a communication means which is dynamically-configurable to selectively arrange communication paths. In other words, Jennings is merely seen to describe altering the processing, i.e., integer versus floating point processing, performed by the processing units, but is not seen to in any way show dynamically configuring a communication means to selectively arrange communication paths for packetized information between processing units. In this regard, each of the configurations shown in Figures 1 to 4 of Jennings is seen to be fixed without any capability to alter the communication paths between the programmable circuit and the processing units.

In addition to the above-noted deficiencies, it is conceded in the Office Action that Jennings fails to show a second distinct configuration of communication paths, which has a deeper pipeline depth than a first configuration. The Office Action relies on Chamdani for this feature.

However, Chamdani is not seen to remedy the deficiencies noted with respect to Jennings. More particularly, while Chamdani describes pipelines of different sizes, Chamdani is not seen to disclose or to suggest an arrangement by which a communication means is configurable to interconnect a plurality of processing units so as

to arrange the processing units in at least two distinct configurations. The cited portion of Chamdani, i.e., col. 32, lines 19 to 38, is seen to describe a fixed processor configuration, which is not seen to in any way provide for dynamic configuration of a communication means to selectively arrange processing units in different and distinct configurations. Nothing in the cited portion of Chamdani is seen to disclose or to suggest a communication means dynamically configurable to selectively arrange communication paths for packetized information between the plurality of processing units of a computer processor over a common bus in at least two distinct configurations, one of which has a deeper pipeline depth than the other.

In addition to the deficiencies noted in the Office Action with respect to Jennings, the Office Action concedes that neither Jennings nor Chamdani show a communication means of a computer processor which includes a common bus. However, the Office Action contends, at page 3, that Oliver discloses a common bus, and that it would have been obvious to alter the teachings of both Jennings and Chamdani to use the common bus described in Oliver.

However, Oliver is seen to concern telecommunications networks and packet switched data communication. The cited portion of Oliver, i.e., col. 11, lines 11 to 19, is seen to concern the use of a common bus to connect network ports to packet memory for storing network packets, such that packets received via the network ports can be stored in the packet memory. Nothing in Oliver is seen to concern a computer processor comprising a dynamically-configurable communication means which includes a common bus to which each of a plurality of processing units of the computer processor are interconnected.

Accordingly, no combination of Jennings, Chamdani and Oliver, if any such combination is even permissible, is seen to show a computer processor comprising a plurality of processing units and a communication means which includes a common bus to which each of a plurality of processing units are interconnected for communication of packetized information over the bus, the communication means being dynamically configurable based on a processing of a computer program to selectively arrange communication paths for packetized information between the plurality of processing units over a common bus in at least two distinct configurations.

Therefore, for at least the foregoing reasons, Claim 1 is believed to be in condition for allowance.

Claim 11 defines data processing method using a computer processor having a plurality of processing units interconnected by communication means comprising a step of dynamically configuring the communication means according to a processing of a computer program to thereby selectively arrange the processing units in a plurality of configurations having a different number of said processing units arranged in parallel and a different number of said processing units arranged in pipelined layers.

Based on the above discussion, the applied art, namely Jennings, Chamdani and Oliver, either alone or in any permissible combination, if one even exists, is not seen to disclose or to suggest dynamically configuring a communication means to selectively arrange communication paths for packetized information, over a common bus of the communication means, between a plurality of processing units in a plurality of configurations having a different number of the processing units arranged in parallel and a different number of the processing units arranged in pipelined layers.

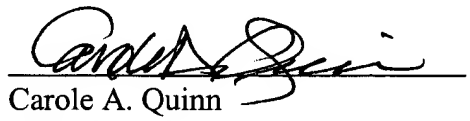
Therefore, for at least the foregoing reasons, Claim 11 is believed to be in condition for allowance.

The remaining claims are each dependent from the independent claims discussed above and are therefore believed patentable for the same reasons. Because each dependent claim is also deemed to define an additional aspect of the invention, however, the individual consideration of each on its own merits is respectfully requested.

In view of the foregoing, the entire application is believed to be in condition for allowance, and such action is respectfully requested at the Examiner's earliest convenience.

Applicant's undersigned attorney may be reached in our Costa Mesa, California office by telephone at (714) 540-8700. All correspondence should be directed to our address given below.

Respectfully submitted,



Carole A. Quinn
Attorney for Applicant
Registration No.: 39,000

FITZPATRICK, CELLA, HARPER & SCINTO
30 Rockefeller Plaza
New York, New York 10112-2200
Facsimile: (212) 218-2200

CA_MAIN 94059v1